IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	: Michail Grinchuk et al.	
Appln. No.:		
Filed	: Herewith	Group Art Unit:
For	: PROCESS FOR DESIGNING COMPARATORS AND ADDERS OF SMALL DEPTH	Examiner:
Docket No.:	01-1060/L13.12-0207	

PRELIMINARY AMENDMENT

Mail Stop New Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the above-identified application as follows:

IN THE CLAIMS

1. (currently amended) A process of implementing logic circuits for logical operations based on a function

$$f_N = x_1 \text{ OR } (x_2 \text{ AND } (x_3 \text{ OR } (x_4 \text{ AND } \ldots x_N \ldots)))$$

or

$$f'_N = x_1 \text{ AND } (x_2 \text{ OR } (x_3 \text{ AND } (x_4 \text{ OR } \ldots x_N \ldots))),$$

comprising steps of:

a) selecting N as the number of ~~inputs~~ variables to the logic circuit; and

b) implementing the logic circuit with two-input gates to a depth between 2n and 2n+2 based on a value of N between 3^n and 3^{n+1}, where n is an integer.

2. (original) The process of claim 1, further including steps of:

c) defining a top portion of the logic circuit based on a

pre-selected pattern of first and second gate types, the top portion defining at least a top level of the circuit and having N inputs and]N/3[outputs,

d) defining a second logic circuit having the same number of inputs as the number of outputs of the top portion, and

e) defining the inputs of the second logic circuit as coupled to the outputs of the top portion.

3. (currently amended) The process of claim 1, further including steps of:

c) transforming groups of three ~~inputs~~ variables of the function into new groups having at most two variables each,

~~d) moving one variable from each group to the next group,~~

~~e~~d) replacing each ~~resulting~~ new group with a single new variable,

~~f~~e) defining a portion of the logic circuit in two-input gates of first and second gate types based on the new variables, the portion having a depth of no more than two levels of the logic circuit, and

~~g~~f) iteratively repeating steps (c) to (~~f~~e) until there are no more than four variables.

4. (original) The process of claim 3, wherein the portion defined during a first iteration defines a top level of the circuit having N inputs and]N/3[outputs, and each portion defined during successive iterations has the same number of inputs as the number of outputs of the portion defined during the next prior iteration and one-third (rounded up to the nearest integer) that number of outputs.

5. (original) The process of claim 3, further including selecting a bottom portion of the logic circuit based on the

number of variables remaining when there are not more than four variables.

6. (original) The process of claim 3, further including steps of:

c) designing the logic circuit with N' inputs, where N' equals 3^n or $2*3^n$,

d) setting odd-positioned inputs to a first binary value and even-positioned inputs to a second binary value in the N'-N most significant inputs, and

e) removing gates that do not contribute to the function.

7. (original) The process of claim 1, further including steps of:

c) for a predetermined value of N, designing a first logic circuit having N-1 inputs and a pre-selected pattern of first and second gate types, the first logic circuit having a portion receiving I-1 most-significant input where I is smaller than N-1, and

d) substituting a predetermined logic circuit having I inputs for the portion of the first logic circuit.

8. (original) The process of claim 7, wherein portions of the logic circuit are defined iteratively, the portion defined during a first iteration being a top level having N-1 inputs and](N-1)/3[outputs, and each portion defined during subsequent iterations having the same number of inputs as the number of outputs of the portion defined during the next prior iteration and one-third that number of outputs.

9. (original) The process of claim 8, further including selecting a bottom portion based on the number of variables remaining when there are no more than four variables.

10. (original) The process of claim 7, wherein the depth of the circuit is

2n, if $3^n < N \leq 3^n+3^{n-2}+3^{n-4}+\ldots$,

2n+1, if $3^n+3^{n-2}+3^{n-4}+\ldots < N \leq 2*3^n+3^{n-2}+3^{n-4}+\ldots$,

2n+2, if $2*3^n+3^{n-2}+3^{n-4}+\ldots < N \leq 3^{n+1}$.

11. (original) The process of claim 1, further including steps of:

c) designing the logic circuit with N′ inputs, where N′ > N and is 3^n or $2*3^n$,

d) setting odd-positioned inputs to a first binary value and even-positioned inputs to a second binary value in the N′-N most significant inputs, and

e) removing gates that do not contribute to the function.

12. (currently amended) A logic~~Logic~~ circuit~~s~~ for performing logical operations designed by the process of claim 1.

13. (currently amended) A computer useable medium having a computer readable program embodied therein for addressing data to design a logic circuit for a function

$$f_N = x_1 \text{ OR } (x_2 \text{ AND } (x_3 \text{ OR } (x_4 \text{ AND } \ldots x_N\ldots)))$$

or

$$f'_N = x_1 \text{ AND } (x_2 \text{ OR } (x_3 \text{ AND } (x_4 \text{ OR } \ldots x_N\ldots))),$$

~~as well as for another logical operations, such as comparison, addition, subtraction and similar that use these functions,~~ where AND and OR represent two-input AND and OR gates, respectively, and N is the number of logical variables of the function, the computer readable program comprising:

first computer readable program code for causing the computer to evaluate N as the number of inputs to the logic

circuit between 3^n and 3^{n+1}, where n is an integer;

second computer readable program code for causing the computer to implement the logic circuit with two-input gates to a depth between 2n and 2n+2 based on a value of N between 3^n and 3^{n+1}, where n is an integer.

14. (original) The computer useable medium of claim 13, further including steps of:

third computer readable program code for causing the computer to define a top portion of the logic circuit based on a pre-selected pattern of first and second gate types, the top portion defining at least a top level of the circuit and having N inputs and]N/3[outputs,

fourth computer readable program code for causing the computer to define a second logic circuit having the same number of inputs as the number of outputs of the top portion, and

fifth computer readable program code for causing the computer to define the inputs of the second logic circuit as coupled to the outputs of the top portion.

15. (currently amended) The computer useable medium of claim 13, further including steps of:

third computer readable program code for causing the computer to transform groups of three ~~inputs~~ variables of the function into new groups having at most two variables each,

~~fourth computer readable program code for causing the computer to move one variable from each group to the next group,~~

~~fifth~~ fourth computer readable program code for causing the computer to replace each ~~resulting~~ new group with a single new variable,

~~sixth~~ fifth computer readable program code for causing the computer to define a portion of the logic circuit in two-input gates of first and second gate types based on the new variables,

the portion having a depths of no more than two levels, and

~~seventh~~ sixth computer readable program code for causing the computer to iteratively execute the third, fourth and~~,~~ fifth ~~and sixth~~ computer readable program codes until there are no more than four variables.

16. (original) The computer useable medium of claim 15, wherein the portion defined during a first iteration defines a top level of the circuit having N inputs and]N/3[outputs, and each portion defined during successive iterations has the same number of inputs as the number of outputs of the portion defined during the next prior iteration and one-third (rounded up) that number of outputs.

17. (original) The computer useable medium of claim 13, further including steps of:

third computer readable program code responsive to a predetermined value of N for causing the computer to design a first logic circuit having N-1 inputs and a pre-selected pattern of first and second gate types, the first logic circuit having a portion receiving I-1 most-significant inputs, where I is smaller than N-1, and

fourth computer readable program code for causing the computer to substitute a second logic circuit having I inputs for the portion of the first logic circuit.

18. (original) The computer useable medium of claim 17, wherein the third computer readable program code includes:

computer readable program code for causing the computer to iteratively define circuit portions based on a pre-selected pattern of first and second gate types, a top portion defining at least a top level of the circuit and having N-1 inputs and](N-1)/3[outputs, and each successive portion having the same

number of inputs as the number of outputs of the portion next higher and having one-third (rounded up) that number of outputs.

19. (original) The computer useable medium of claim 18, further including:

computer readable program code causing the computer to identify a bottom portion for the circuit based on a number of variables remaining when there are no more than four variables.

20. (original) The computer useable medium of claim 13, wherein the computer readable program further includes

third computer readable program code for causing the computer to identify a smallest value of N' > N equal to 3^n or $2*3^n$,

fourth computer readable program code responsive to the value of N' for causing the computer to design the logic circuit with N' inputs,

fifth computer readable program code for causing the computer to set odd-positioned inputs to a first binary value and even-positioned inputs to a second binary value in the N'-N most significant inputs, and

sixth computer readable program code for causing the computer to remove gates that do not contribute to the function.

21. (new) The process of claim 3, further including, before step d),

moving a variable from each group of three variables to the new group.

22. (new) The computer useable medium of claim 15, wherein the third computer readable program code includes

computer readable program code for causing the computer to move a variable from each group of three variables to the new

group.